

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,018,873 B2
APPLICATION NO. : 10/639942
DATED : March 28, 2006
INVENTOR(S) : Hussein I. Hanafi et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page item 57) Abstract, line 1
"provides SOI CMOS"

should read

--The present invention provides SOI CMOS --

Column 11, Line 19, Claim 17:

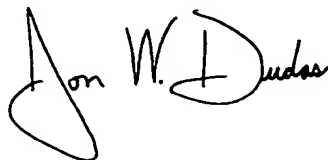
"forming suicide" should read -- forming silicide --

Column 12, Line 20, Claim 19:

"polySi gates and the" should read -- polySi gate and the --

Signed and Sealed this

Eighth Day of August, 2006

A handwritten signature in black ink, appearing to read "Jon W. Dudas". The signature is stylized with a large, looped initial "J" and a distinct "D" at the end.

JON W. DUDAS
Director of the United States Patent and Trademark Office